Remarks/Arguments:

Claims 1-35 and 38-41 are pending and stand rejected.

By this Amendment, claims 1, 17, 27-28, 31-32 and 38-39 are amended and claim 40 is cancelled without prejudice.

No new matter is presented by the claim amendments. Support for the claim amendments can be found though out the original specification and, for example, in the original specification at paragraphs [0037]-[0038].

Examiner Interview

An Examiner Interview was held on May 28, 2009 between Applicant's Representative Eric Berkowitz and Examiner Lam. The Examiner is thanked for his efforts. In the Examiner Interview, Applicant's Representative reviewed a proposed claim 1 with the Examiner. The Examiner suggested that the proposed claim overcame the current rejection, but indicated that another search would be necessary. The Examiner also suggested minor changes to proposed claim 1. Applicant has amended the claim set provided in this Amendment in accordance with the proposed claim discussed with the Examiner.

Rejection of Claims 17-21, 26-35 and 38-40 under 35 U.S.C. §102(b).

In the Office Action, at item 5, claims 17-21, 26-35 and 38-40 are rejected under 35 U.S.C. §102(a) as being anticipated by Shirakawa (U.S. Patent Publication No. 2003/0117501).

Reconsideration is respectively requested.

Claim 17

Claim 17 is directed to an electronic apparatus, and recites:

> ... at the first image module, portions of the first captured image are selectively blocked, based on a window-of-disinterest indicating the portions of the first captured image that are not to be transmitted on the common data line from the first image module, by successively tri-stating a connection between the first image module and the common set of data lines during successive time periods and at the second image module, portions of the second captured image are transmitted on the common set of data lines during the successive time periods by successively tri-stating a connection between the second image module and the common set of data lines, the successive time periods synchronizing the first and second captured images received by the circuitry on the substrate to generate a picture-in-picture image that includes unblocked portions of the first captured image and the transmitted portions of the second captured image.

That is, the unblocked portions of the first captured image and the transmitted portions of the second captured image are synchronized to generate a picture-in-picture image received at circuitry on the substrate. Moreover, the portions of the first and second captured images received by the circuitry are generated by successively tri-stating connections to a common set of data lines and the portions of the first captured image blocked are based on a window-of-disinterest.

Shirakawa Reference

Shirakawa discloses that a Digital Signal Processor (DSP) 3 runs control programs to implement functions of the selector 5, a sensor controller 101, a controller 102 and an image processor 103. The sensor controller 101 of Shirakawa controls the image sensors 2a and 2b under the control of the controller 102. More specifically, in Shirakawa, the image sensors 2a and 2b are driven by the sensor controller 101 to sequentially output background image data Sa and foreground image data Sb in units of a horizontal line to the image processor 103. That is, the selector 5 alternately selects the background image data Sa and the foreground image data Sb on a line-by-line basis (i.e., horizontal line-by-horizontal line). In particular, Shirakawa discloses the selection of an entire line (i.e., the i-th horizontal line of background image data Sa or the i-th horizontal line of foreground image data Sb) to output to the image processor 103. (See Shirakawa at paragraph [0046].) Moreover, Shirakawa discloses in a different embodiment (see Fig. 3C of Shirakawa) that the output from selector 5 may be stored in memory to allow superimposing of the foreground image data Sb onto the background image data Sa by overwritting the background image data Sa in a preset region. (See Shirakawa at paragraphs [0037]-[0038].) That is, Shirakawa cannot receive a picture-in-picture image via synchronization of portions of the first and second image data on the common set of data lines because Shirakawa has no mechanism for controlling data through selector 5 in increments less than one horizontal line. Shirakawa can only achieve a picture-in-picture image by overwritting in memory 6 the background image data Sa using the foreground image data Sb.

Accordingly, claim 17 is submitted to patentably distinguish over Shirakawa for at least the above-mentioned reasons.

Claims 31 and 38

Claims 31 and 38, which include similar but not identical features to those of claim 17, are submitted to patentably distinguish over Shirakawa for at least the same reasons as claim 17.

Claim 40

Claim 40 is cancelled without prejudice. Accordingly the rejection of claim 40 is now moot.

Claims 18-21, 26-30, 32-35 and 39

Claims 18-21, 26-30, 32-35 and 39, which include all of the limitations of claim 17, 31 or 38, are submitted to patentably distinguish over Shirakawa for at least the same reasons as their respective independent claims.

Rejection of Claims 1-7, 11-16 and 41 under 35 U.S.C. §103(a)

In the Office Action, at item 6, claims 1-7, 11-16 and 41 are rejected under 35 U.S.C. §103(a) as unpatentable over Shirakawa in view of Miyake (U.S. Patent Publication No. 2001/0050721).

Reconsideration is respectively requested.

Claim 1

Claim 1, which include similar but not identical features to those of claim 17, is submitted to patentably distinguish over Shirakawa for at least the same reasons as claim 17.

Claims 2-7, 11-16 and 41

Claims 2-7, 11-16 and 41, which include all of the limitations of claim 1, are submitted to patentably distinguish over Shirakawa for at least the same reasons as claim 1.

Miyake Reference

The addition of Miyake does not overcome the deficiencies of Shirakawa. This is because, Miyake, which is used by the Examiner to teach a dual camera module that is attached to a flex printed circuit or connector, does not disclose or suggest "successively tri-stating a connection between the first [or second] image module and the common data line" and, furthermore, generation of "a picture-in-picture image that includes unblocked portions of the captured first image data and the transmitted portions of the second image data," (brackets added) as required by claim 1.

Accordingly, claim 1 and dependent claims 2-7, 11-16 and 41 by virtue of their dependency on claim 1, are submitted to patentably distinguish over Shirakawa in view of Miyake for at least the above-mentioned reasons.

Rejection of Claims 8 and 10 under 35 U.S.C. §103(a)

In the Office Action, at item 7, claims 8 and 10 are rejected under 35 U.S.C. §103(a) as unpatentable over Shirakawa in view of Miyake in further view of Johnson (U.S. Patent Publication No. 2006/0197847).

Reconsideration is respectively requested.

Claims 8 and 10, which include all of the limitations of claim 1, are submitted to patentably distinguish over Shirakawa in view of Miyake for at least the same reasons as claim 1.

Johnson Reference

The addition of Johnson does not overcome the deficiencies of Shirakawa and Miyake. This is because, Johnson, which is used by the Examiner to teach an image processor system wherein an I2C bus is used, does not disclose or suggest "successively tri-stating a connection between the first [or second] image module and the common data line" and, furthermore, generation of "a picture-in-picture image that includes unblocked portions of the captured first image data and the transmitted portions of the second image data," (brackets added) as required by claim 1.

Accordingly, claims 8 and 10 are submitted to patentably distinguish over Shirakawa in view of Miyake in further view of Johnson for at least the above-mentioned reasons.

Rejection of Claims 9 and 22-25 under 35 U.S.C. §103(a)

In the Office Action, at item 8, claims 9 and 22-25 are rejected under 35 U.S.C. §103(a) as unpatentable over Shirakawa in view of Miyake in further view of Stam (U.S. Patent Publication No. 2004/0230358).

Reconsideration is respectively requested.

Claims 9 and 22-25, which include all of the limitations of claim 1 or claim 17, are submitted to patentably distinguish over Shirakawa in view of Miyake for at least the same reasons as claim 1 or claim 17.

Stam Reference

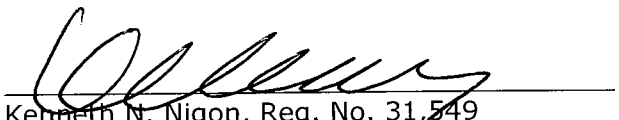
The addition of Stam does not overcome the deficiencies of Shirakawa and Miyake. This is because, Stam, which is used by the Examiner to teach a flex interconnect that includes a Serial Peripheral Interface (SPI), does not disclose or suggest "successively tri-stating a connection between the first [or second] image module and the common data line" and, furthermore, generation of "a picture-in-picture image that includes unblocked portions of the captured first image data and the transmitted portions of the second image data," (brackets added) as required by claim 1.

Accordingly, claims 9 and 22-25 are submitted to patentably distinguish over Shirakawa in view of Miyake in further view of Stam for at least the above-mentioned reasons.

Conclusion

In view of the claim amendments and remarks, Applicant submits that the application is in condition for allowance, which action is respectfully requested.

Respectfully submitted,



Kenneth N. Nigon, Reg. No. 31,549
Eric Berkowitz, Reg. No. 44,030
Attorneys for Applicant

KNN/EB/

Dated: June 19, 2009

P.O. Box 980
Valley Forge, PA 19482
(610) 407-0700

The Director is hereby authorized to charge or credit Deposit Account No. **18-0350** for any additional fees, or any underpayment or credit for overpayment in connection herewith.

S_H:\NRPORTBL\RP\SSEILER\442199_1.DOC